WHAT IS CLAIMED IS:

1. An apparatus comprising:

a first storage location configured to store a segment selector identifying a segment descriptor including a first operating mode indication and a second operating mode indication;

a second storage location configured to store an enable indication, wherein said enable indication, said first operating mode indication, and said second operating mode indication are indicative of an operating mode; and

a processor configured to process an instruction according to said operating mode.

2. The apparatus as recited in claim 1 wherein said operating mode is a first operating mode if said enable indication is in an enabled state and said first operating mode indication is in a first state, and wherein said operating mode is a second operating mode if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state.

3. The apparatus as recited in claim 2 wherein said second operating mode is one of a plurality of operating modes available if said enable indication is in said enabled state and said first operating mode indication is in said second state, and wherein said one of said plurality of operating modes is selected in response to a state of said second operating mode indication.

4. The apparatus as recited in claim 3 wherein one of said plurality of operating modes is a 32 bit operating mode.

5. The apparatus as recited in claim 3 wherein one of said plurality of operating modes is a 16 bit operating mode.

6. The apparatus as recited in claim 2 wherein said first operating mode includes a default address size which is greater than 32 bits.

7. The apparatus as recited in claim 6 wherein said first operating mode further includes a default operand size of 32 bits.

8. The apparatus as recited in claim 2 wherein said segment descriptor is one of a plurality of segment descriptors stored in a descriptor table including a plurality of entries, and wherein at least one of said plurality of segment descriptors occupies two of said plurality of entries.

9. The apparatus as recited in claim 8 wherein said one of said plurality of segment descriptors is a call gate descriptor.

10. The apparatus as recited in claim 8 wherein said one of said plurality of segment descriptors is an interrupt gate descriptor.

11. The apparatus as recited in claim 8 wherein said one of said plurality of segment descriptors is a trap gate descriptor.

12. The apparatus as recited in claim 8 wherein said one of said plurality of segment descriptors is a task state segment descriptor.

13. The apparatus as recited in claim 8 wherein said one of said plurality of segment descriptors is a local descriptor table descriptor.

14. The apparatus as recited in claim 1 wherein said first storage location is a memory location.

15. The apparatus as recited in claim 1 wherein said first storage location is a general purpose register within said processor.

16. The apparatus as recited in claim 1 wherein said first storage location is a special purpose register within said processor.

17. The apparatus as recited in claim 1 wherein said second storage location is a memory location.

18. The apparatus as recited in claim 1 wherein said second storage location is a general purpose register within said processor.

19. The apparatus as recited in claim 1 wherein said second storage location is a special purpose register within said processor.

20. The apparatus as recited in claim 1 wherein said processor is configured to process said instruction by executing interpreter software which emulates said instruction.

21. The apparatus as recited in claim 1 wherein said processor is configured to process said instruction by executing translation software to translate said instruction into one or more native instructions to be executed by said processor.

22. The apparatus as recited in claim 1 wherein, if said enable indication is in a disabled state, said first operating mode indication is undefined and said second operating mode indication is indicative of said operating mode.

23. A method comprising:

determining an operating mode in response to an enable indication in a first storage location, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor;

fetching operands and generating addresses in response to said operating mode.

24. The method as recited in claim 23 wherein said determining comprises determining a first operating mode responsive to said enable indication being in an enabled state and said first operating mode indication being in a first state, and wherein said first operating mode includes a default address size greater than 32 bits.

25. The method as recited in claim 24 wherein said first operating mode includes a default operand size of 32 bits.

26. The method as recited in claim 23 wherein said segment descriptor is one of a plurality of segment descriptors stored in a descriptor table having a plurality of entries, the method further comprising reading a second segment descriptor of said plurality of segment descriptors from said segment descriptor table, wherein said second segment descriptor occupies up to two entries of said plurality of entries depending upon a type of said second segment descriptor.

27. The method as recited in claim 26 wherein said second segment descriptor is a call gate descriptor.

28. The method as recited in claim 26 wherein said second segment descriptor is an interrupt gate descriptor.

29. The method as recited in claim 26 wherein said second segment descriptor is a trap gate descriptor.

30. The method as recited in claim 26 wherein said second segment descriptor is a task state segment descriptor.

31. The method as recited in claim 26 wherein said second segment descriptor is a local descriptor table descriptor.

32. The method as recited in claim 24 wherein said determining further comprises determining a second operating mode responsive to said enable indication being in an enabled state, said first operating mode indication being in a second state, and said second operating mode being in said first state, and wherein said first operating mode includes a default address size of 32 bits.

33. The method as recited in claim 24 wherein said determining further comprises determining one of a plurality of operating modes if said enable indication is in said enabled state and said first operating mode indication is in a second state, and wherein said one of said plurality of operating modes is selected in response to a state of said second operating mode indication.